V6363
(CMDC)

■ OUTLINE

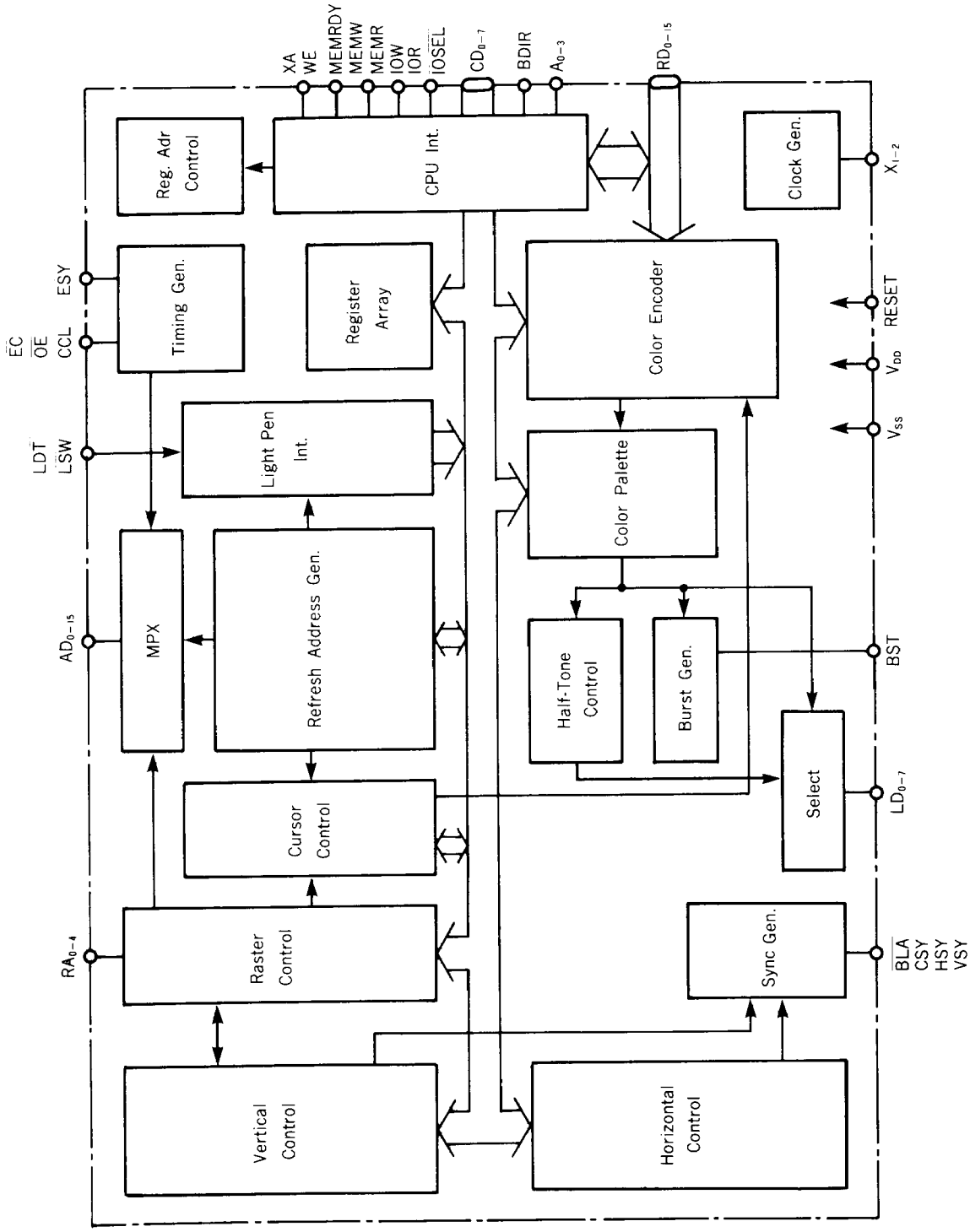
The CMDC is compatible with the CGA (Color Graphics Adapter), MDA (Monochrome Display Adapter), and HGC (Hercules Graphics Card), all for IBM PC application. In case the software and hardware for connecting a regular monitor come as a pair, the CMDC offers compatibility without requiring software changes (initialization is also unnecessary). Even in case of connecting different monitors, initialization will only be performed once at Power Start-Up, then compatibility will be available without requiring any software changes. It is thus possible, for example, to run CGA software using an IBM monochrome monitor. (A gray scaling/hatching display can be used with a monochrome monitor.)

Because the CMDC has the display capacity of the IBM PC as well as numerous other expansion functions, including Kanji display, Color Palette, a high-performance display system can be easily configured.

■ FEATURES

- All functions of MC6845 are built in (excluding the Interlacing & Video Mode and the Skew function).
- A gray scaling/hatching display can be used with a monochrome monitor.
- IBM PC software for 640 by 200 PELs can be directly displayed on a 640 by 400 PEL screen. (An 8 by 16 character font can be used, and can be displayed even in Double Scan Mode.)
- In addition to the standard IBM PC Graphics Modes, a variety of other Graphics Modes are provided: 320 by 200 PELs x 16 or 256 colors, 320 by 400 PELs x 4 or 16 colors, 640 by 200 PELs x 4 or 16 colors, 640 by 400 PELS x 4 colors, 640 by 350 PELs x 16 colors, and so on.
- A Protect Bit is provided for software protection.
- An SRAM or DRAM can be used as the VRAM. (Because the timing for display and the CPU are separate, the CPU can access VRAM at any time (without awaiting the retrace-timing.))
- Built-in interface for the Light Pen
- With a linear RGB monitor, 16 out of 512 colors can be simultaneously displayed.
- With an EGA monitor, 16 out of 64 colors can be simultaneously displayed.
- A Color Lookup Table can even be used with an IBM color monitor.
- A Standby function is provided to conserve power dissipation.
- Kanji display capacity of 16 by 16, 24 by 24 or 32 by 32 "PELs" (picture elements or pixels). (Attributes can also be used).
- The font configuration can be selected. Horizontal: 6, 7, 8, 9, 10, or [8 x integer] PELs (capable of a mixed display of half-width and full-width text); Vertical: 1 to 32 PELs.
- Capable of smooth scrolling and (in Non-interlace Mode only) external synchronization
- CMOS, 5V power supply, 100-pin QFP or 84-pin PLCC

■ BLOCK DIAGRAM



■ DESCRIPTION OF TERMINAL FUNCTIONS

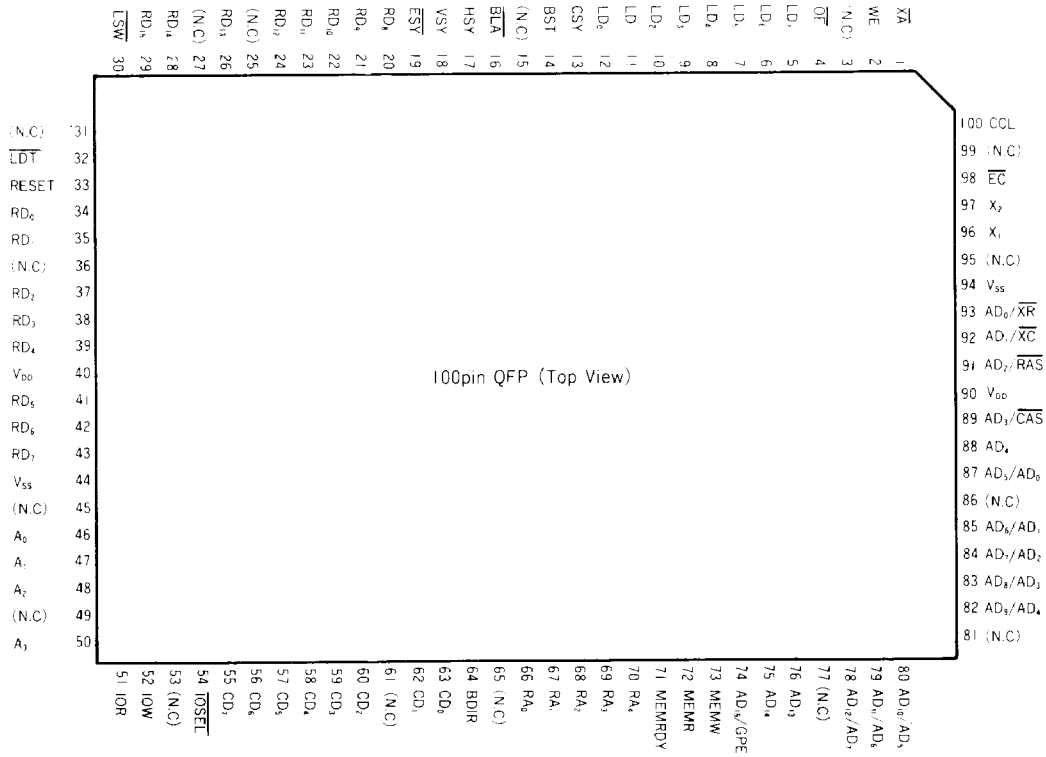
Signal Name	I/O	Terminal Functions
A_0	I	Address for I/O register selection. A_0 is also used for selecting the high or low byte.
⌇		
A_3	I	
CD_0	I/O	Data Bus for the CPU
⌇		
CD_7	I/O	
MEMRDY	O	Read/Write Ready signal for the Memory ("0": Wait)
MEMW	I	Controls writing to Memory
MEMR	I	Controls reading from Memory
IOW	I	Controls writing to the I/O registers
IOR	I	Controls reading from the I/O registers
$\overline{\text{IOSEL}}$	I	Enable signal to the I/O Register D and E ("0": Enable)
RESET	I	Reset signal
$\overline{\text{LSW}}$	I	Light Pen Switch signal (At RESET, specifies an 8- or 16-bit Data Bus for VRAM)
$\overline{\text{LDT}}$	I	Light Pen Detection signal (At RESET, specifies VRAM from SRAM or DRAM)
X_1	I	For X'tal oscillation or external clock input
X_2	I/O	
BDIR	O	Direction control of the bi-direction buffer for the CPU Data Bus
RA_0	O	Raster Address
⌇		
RA_3	O	
RA_4	I/O	Raster Address (At RESET, specifies the Hercules or CGA Mode)
RD_0	I/O	Data bus for VRAM (Low side)
⌇		
RD_7	I/O	
RD_8	I/O	Data bus for VRAM (High side)
⌇		
RD_{15}	I/O	
$\overline{\text{EC}}$	O	Transmission control for the RD Bus of Character Font Data
$\overline{\text{OE}}$	O	Output control (for SRAM)
CCL	O	Latch clock for character codes
$\overline{\text{WE}}$	O	Controls writing of VRAM
$\overline{\text{XA}}$	O	CPU-related timing for VRAM
V_{SS}	I	0V
V_{SS}	I	
V_{DD}	I	+5V
V_{DD}	I	

Signal Name	I/O	Terminal Functions					
AD0/$\overline{XR}$	O	Addresses of SRAM			Addresses of DRAM		CPU RAS Address timing for DRAM
AD1/$\overline{XC}$	O						CPU CAS Address timing for DRAM
AD2/$\overline{RAS}$	O						$\overline{RAS}$ for DRAM
AD3/$\overline{CAS}$	O						$\overline{CAS}$ for DRAM
AD4	O						
AD5/AD0	O						
AD6/AD1	O						
AD7/AD2	O						
AD8/AD3	O						
AD9/AD4	O						
AD10/AD5	O						
AD11/AD6	O						
AD12/AD7	O						
AD13	O						
AD14	O						
AD15/GPE	O	Also, OR output of Bits 0 and 1 of the Control Register in Hercules Mode					
LD4	O	DB	for IBM color monitor	Primary	B	for EGA monitor	B0
LD5	O	DG		Primary	G		B1
LD6	O	DR		Primary	R		B2
LD7	O	DI		Secondary	G		G0
LD0	O	$\overline{BFP}$		←			←
LD1	O						G1
LD2	O			Secondary	R		G2
LD3	O	Video		Secondary	B		R0
$\overline{BLA}$	O	$\overline{BLANK}$		←			R1
BST	O	Color Burst		←			R2
CSY	O	Composite Sync		←			←
HSY	O	Horizontal synchronization		←			←
VSY	O	Vertical synchronization		←			←
$\overline{ESY}$	I/O	for external synchronization					

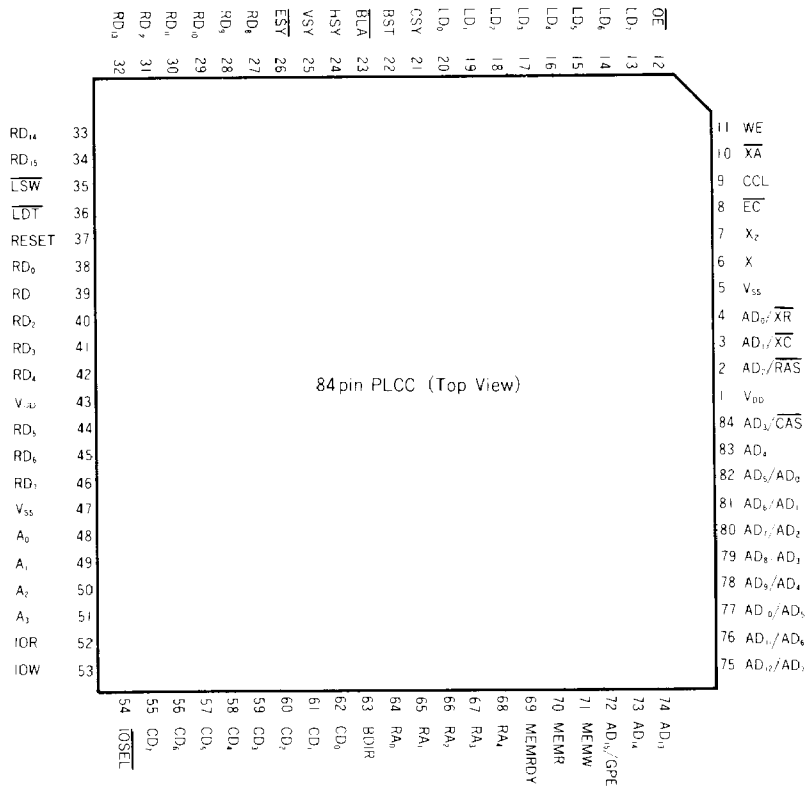
for linear RGB monitor

■ PIN ASSIGNMENT

(1) 100pin QFP



(2) 84pin PLCC



■ ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Supply voltage	V_{DD}	−0.3	+7.0	V
Input voltage	V_I	−0.3	V_{DD}+0.3	V
Output voltage	V_O	−0.3	V_{DD}+0.3	V
Operating temperature	T_{OP}	0	+70	°C
Storage temperature	T_{STG}	−50	+125	°C

(Based on the reference voltage of Vss=0.0V)

Recommended Condition for Use

Supply voltage: +5V±5% (based on Vss=0.0V)
Operating temperature: 0~70°C

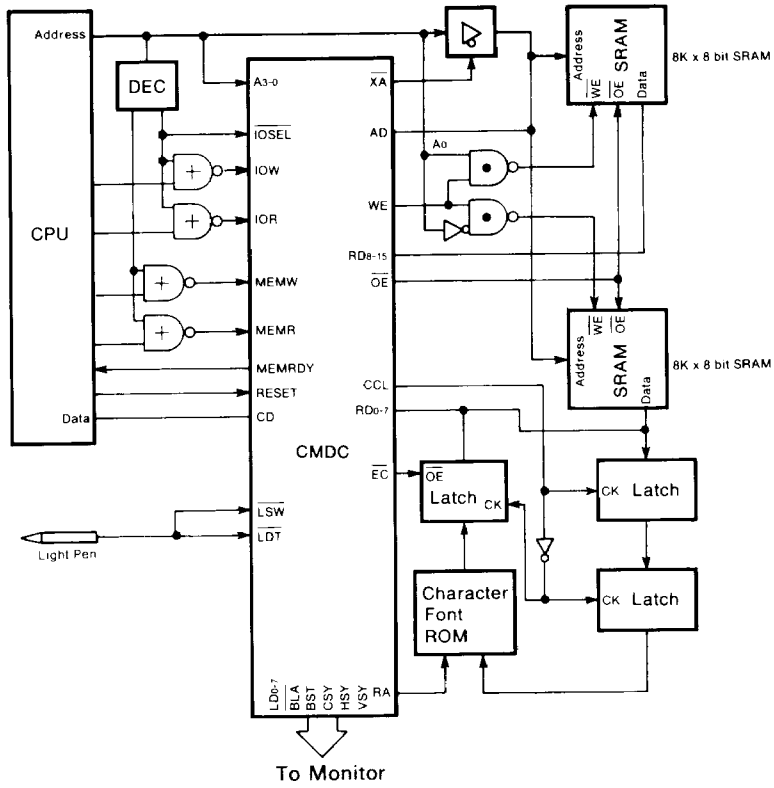
DC Characteristics (V_{DD}=5V±5%, T_{OP}=0~70°C)

Item	Symbol	Condition	Min.	Max.	Unit
High-level output voltage (for TTL driving)	V_{OH}	I_{OH}=−0.4mA	2.7		V
Low-level output voltage (for TTL driving)	V_{OL}	I_{OL}=0.8mA		0.4	V
High-level output voltage (for CMOS driving)	V_{OH}	$\|I_{OH}\|$<10μA	V_{DD}−0.4		V
Low-level output voltage (for CMOS driving)	V_{OL}	$\|I_{OL}\|$<10μA		0.4	V
High-level input voltage	V_{IH}		2.2		V
Low-level input voltage	V_{IL}			0.8	V
Input leak current	I_L		−10	10	μA
OFF status leak current	I_{LZ}		−10	10	μA
Power current (during normal operation)	I_{DD}			70	mA
Power current (during Standby)	I_{DD}			10	mA

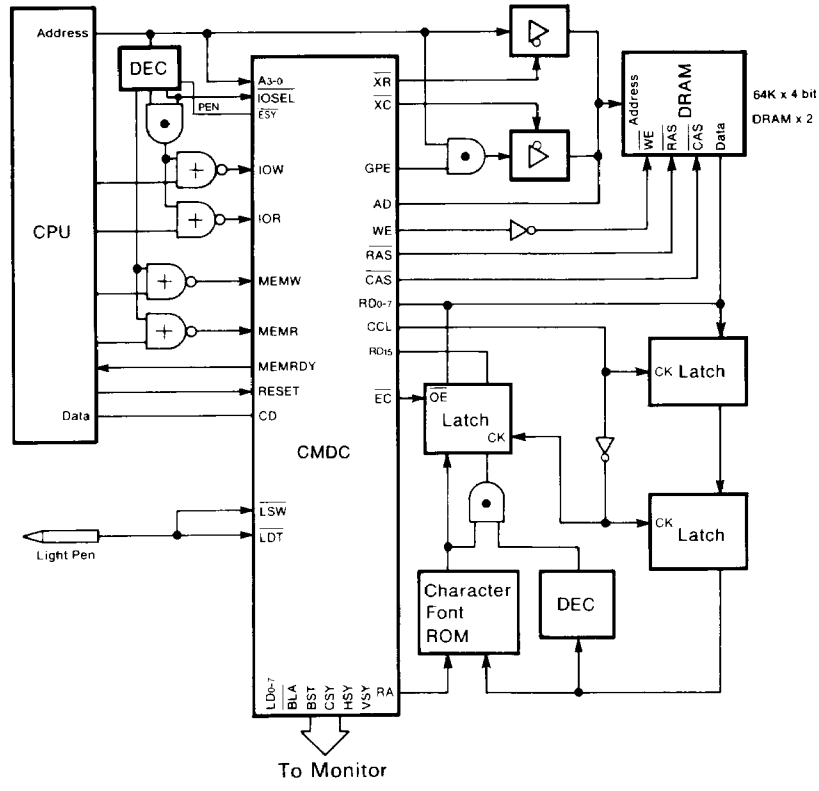
NOTE: ILZ applies while the CD0-CD7, RD0-RD15, X2, RA4, or $\overline{ESY}$ pins are in input status or while the AD0/$\overline{XR}$ ~ AD15/GPE or MEMRDY pins are in high-impedance status.

■ SYSTEM CONFIGURATIONS

(1) Use of SRAM (For 16-Bit Bus, CGA)

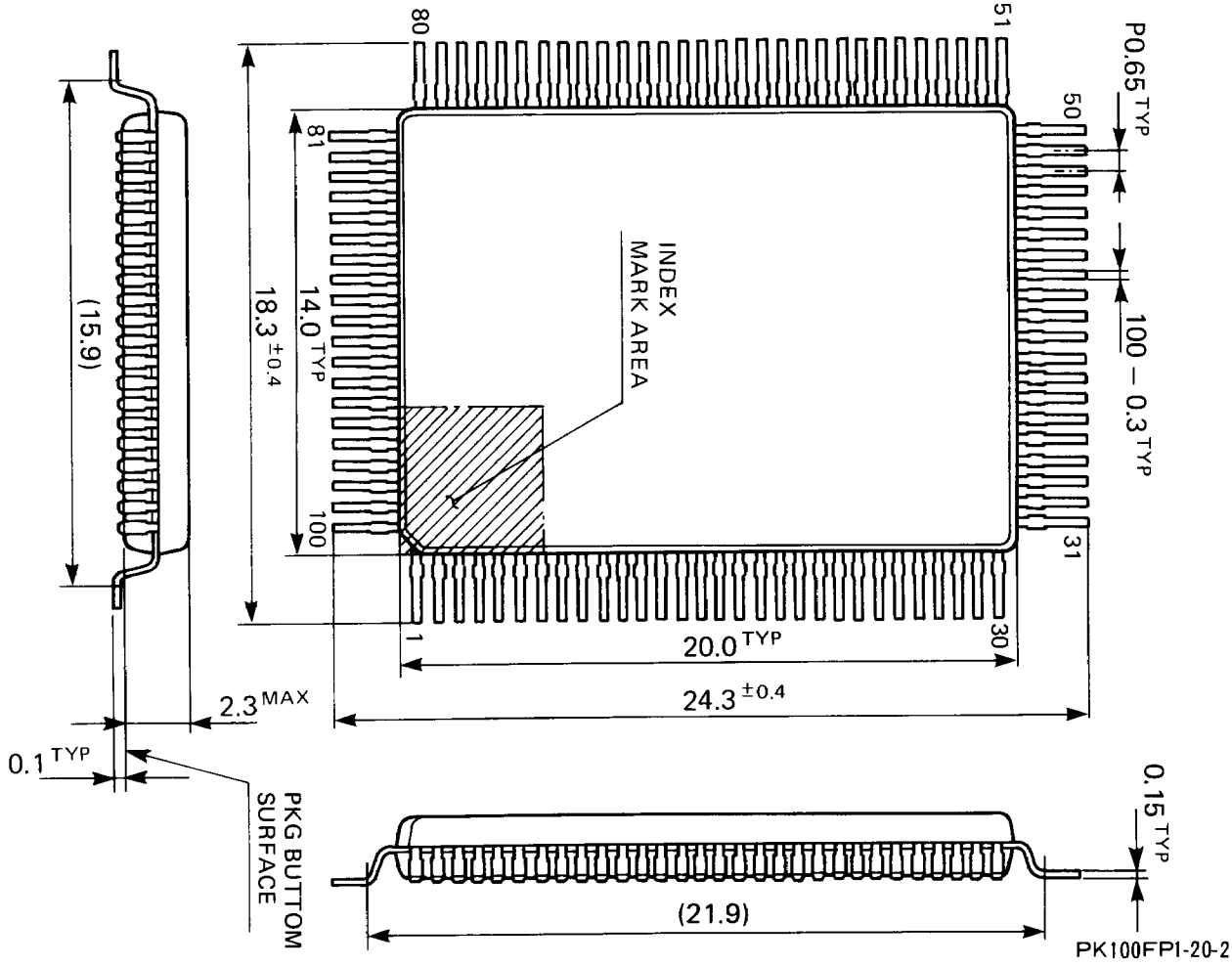


(2) Use of DRAM (For 8-Bit Bus, Hercules)

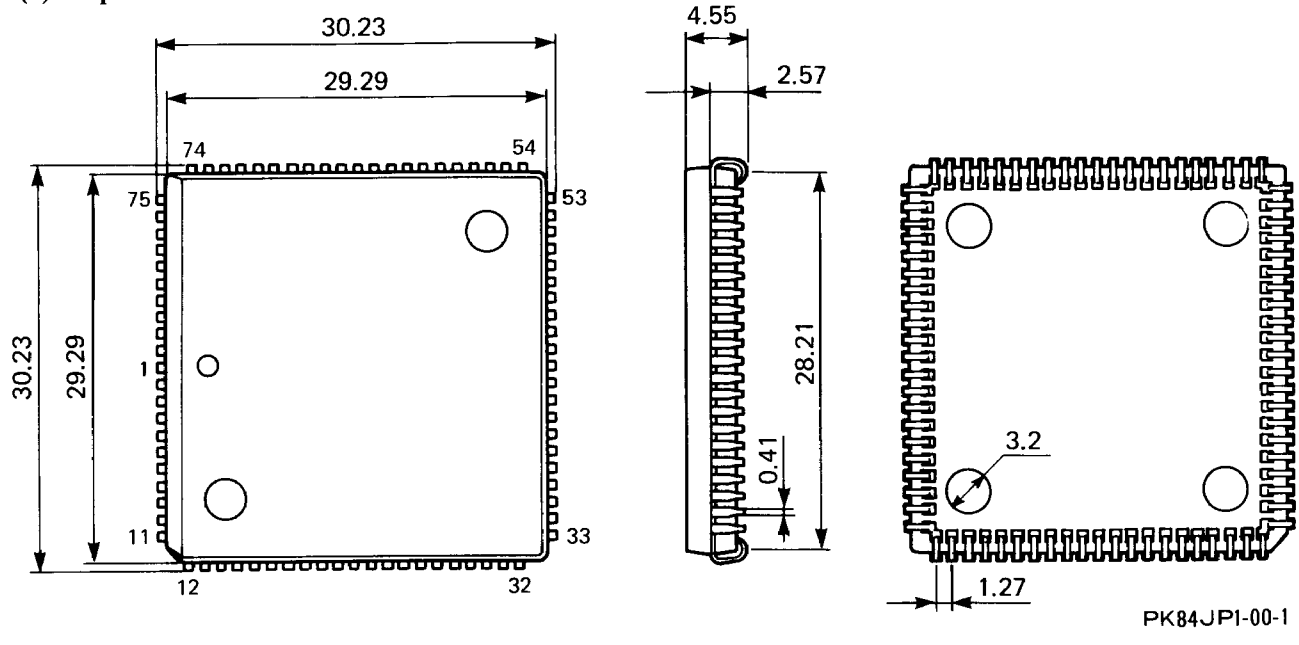


■ PACKAGE OUTLINES

(1) 100pin QFP



(2) 84pin PLCC



The specifications of this product are subject to improvement changes without prior notice.

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